

Dr. Annu Kumari

Dept. of Physics

H. D. Jain College, Ara

Ph sem III

Paper - CC12

Unit - 1

Topic :- 555 IC Timer

# The 555 IC timer

The 555 timer is an IC timer device. It can operate both as monostable and astable multivibrator. This monolithic device has advantages over discrete circuits of monostable and astable multivibrator. It has fewer circuit connections and provides improved performance. It generates a pulse whose width can be varied by varying externally connected resistance and capacitance ( $R$  and  $C_T$ ).

## Circuit of the 555 timer :-

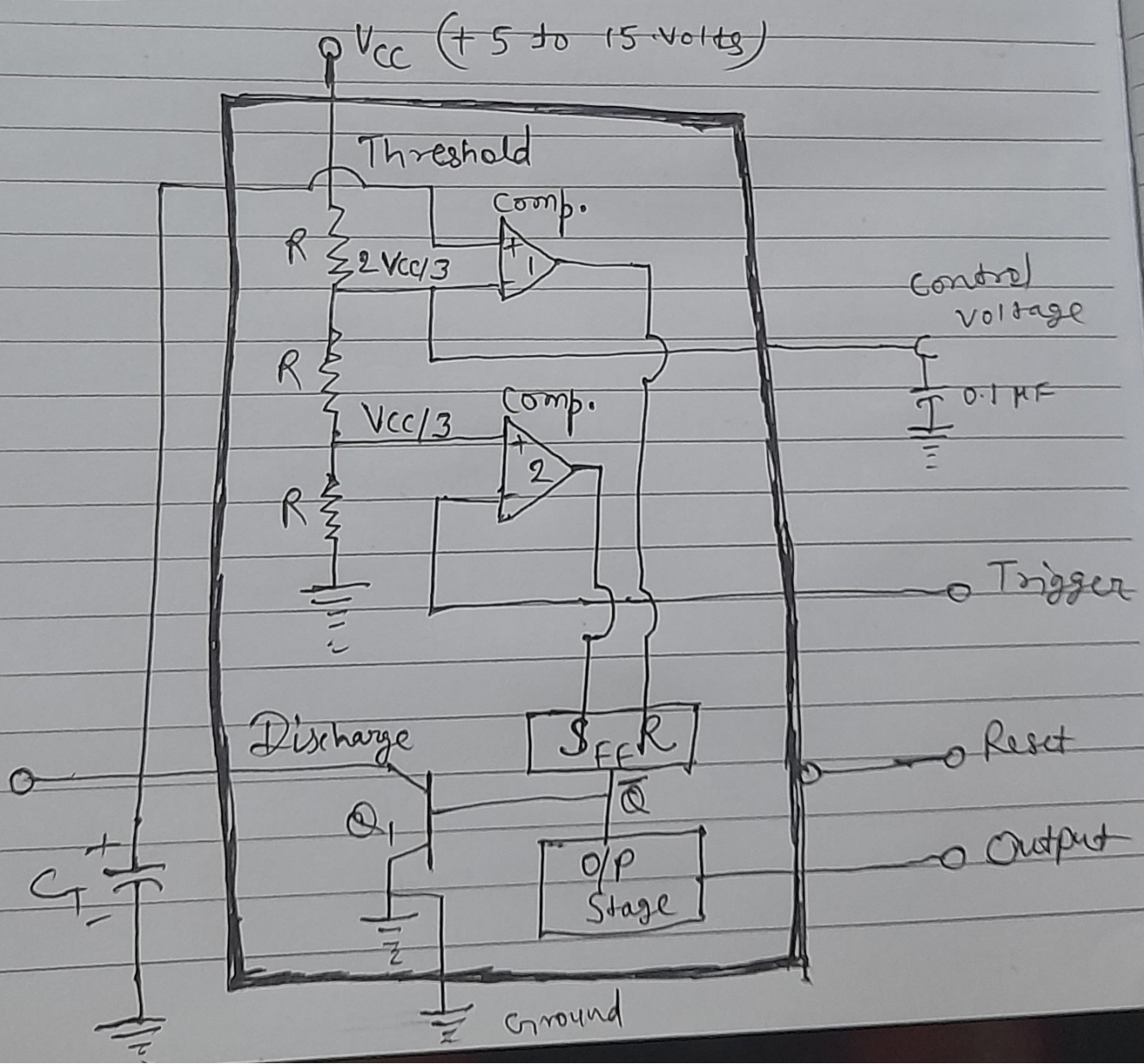


fig ① functional diagram of the type 555 IC timer.

It can operate as an ~~astable~~ multivibrator or it can be triggered externally for monostable mode of operation. It has three inputs: Threshold; Trigger and Reset. These inputs control the states of the output terminal and discharge terminal. The output of the flip flop is  $\bar{Q}$  which is also used as an output terminal taken through an output stage fig ①. The three equal resistances  $R$  establish reference voltage levels  $V_1 = \frac{2V_{CC}}{3}$  for comparator - 1 and  $V_2 = \frac{V_{CC}}{3}$

for comparator - 2. These reference levels are required to control the timing as explained below.

(i) SET state of FF (flip flop): On a negative transition of pulse applied at the trigger terminal and when the voltage at the trigger terminal passes through  $V_{CC}/3$ , the output of the comparator - 1 changes state because its positive input terminal is fixed at  $V_{CC}/3$ . This change of state

sets the flip flop (FF). The output at the output terminal is high. (logic-1 state). (A)

(ii) Reset state of FF: - When voltage applied at the threshold terminal of comparator - 1 goes positive and passes through reference level  $\frac{2V_{CC}}{3}$ , the

output of comparator - 1 changes state. This change of state resets the flip flop. The output at the output terminal is low (logic-0 state). A separate reset terminal is provided for the timer and is used to reset the flip flop externally.

Since a high current of the order of 200 mA is sourced by the output stage a capacitor  $C_T$  is connected between discharge T terminal and ground. When  $Q_1$  is OFF, the capacitor charges and when  $Q_1$  is ON it discharge quickly,  $C_T$ . The top of  $C_T$  is also connected to threshold

so that capacitor voltage is applied to the threshold input.